CLAIMS

WHAT IS CLAIMED:

1. A circuit for performing a voltage level translation, said circuit comprising:

a transistor circuitry for receiving an input signal for translating a signal from a first voltage range to a second voltage range; and

a first one-shot and a second one-shot operatively coupled to said transistor circuitry, said first and second one-shots to provide at least one pulse for translating said input signal from said first voltage range to said second voltage range.

2. The circuit of claim 1, wherein said transistor circuitry further comprises a voltage level translator, comprising:

a first transistor operatively coupled to said input signal, said input signal being in said first voltage range, wherein said first one-shot circuit is being driven by said first transistor;

a second transistor to receive a complementary signal of said control signal, said second transistor to drive a second one-shot circuit to provide a second pulse; and

a first pair and a second pair of transistors, each pair being operatively coupled to said first and second transistors, said first and second pairs of transistors to provide a transition of a signal from a first voltage range to a second voltage range.

3. The circuit of claim 2, wherein said first voltage range relates to a voltage of V_{CC} to ground.

4. The circuit of claim 2, wherein said second voltage range relates to a voltage of V_{CC} to V_{BB}.

5. The circuit of claim 2, wherein said voltage level translator is a negative voltage translator.

6. The circuit of claim 5, wherein said first and second transistors are P-channel transistors.

7. The circuit of claim 6, wherein the drain terminals of said first and second transistors are coupled to V_{CC}.

8. The circuit of claim 5, wherein said first pair of transistors are N-channel transistors.

9. The circuit of claim 6, wherein the source terminals of said first pair of transistors are respectively coupled to said drain terminals of said first and second transistors.

10. The circuit of claim 9, wherein the drain terminals of said second pair of transistors are respectively coupled to the source terminals of said first pair of transistors.

11. The circuit of claim 6, wherein said source terminals of said second pair of transistors are coupled to said second voltage level, said second pair of transistors being N-channel transistors.

12. The circuit of claim 6, wherein said second voltage level is V_{BB}.

13. The circuit of claim 6, wherein said first voltage level is ground.

14. The circuit of claim 6, wherein said first and second one-shots each provide a low-going pulse.

15. The circuit of claim 2, wherein said first one-shot further comprises:

a first inverter to receive a first control signal from said first transistor;

a second inverter operatively coupled to said first inverter;

a first N-channel transistor comprising a well tie to said second voltage level, the source terminal of said first N-channel transistor being coupled to said first control signal; and

a second N-channel transistor comprising a well tie to said second voltage level, said second N-channel transistor being coupled with said first P-channel transistor, the gate of said second N-channel transistor being coupled to said input signal.

16. The circuit of claim 2, wherein said second one-shot further comprises:

a third inverter to receive a first control signal from said first transistor;

a fourth inverter operatively coupled to said third inverter;

a third N-channel transistor comprising a well tie to said second voltage level, the source terminal of said first N-channel transistor being coupled to said first control signal; and

a fourth N-channel transistor comprising a well tie to said second voltage level, said fourth N-channel transistor being coupled with said third N-channel transistor, the gate of said fourth N-channel transistor being coupled to said a complement of said input signal.

17. The circuit of claim 16, wherein said second one-shot provides an output signal that is in said second voltage range.

18. The circuit of claim 2, wherein said first and second transistors are N-channel transistors.

19. The circuit of claim 18, wherein said first and second pair of transistors are P-channel transistors.

20. The circuit of claim 19, wherein said first and second one-shots each provide a high-going pulse.

21. A voltage level translator, comprising:

a first transistor operatively coupled to a control signal, said control signal being in a first voltage range;

a first one-shot circuit driven by said first transistor, said first one-shot circuit to provide a pulse;

a second transistor to receive a complementary signal of said control signal;

a first pair and a second pair of transistors, each pair being operatively coupled to said first and second transistors, said first and second pairs of transistors to provide a transition of a signal from a first voltage range to a second voltage range.

22. The voltage level translator of claim 21, wherein said first voltage range relates to a voltage of V_{CC} to ground.

23. The voltage level translator of claim 21, wherein said second voltage range relates to a voltage of V_{CC} to V_{BB}.

24. The voltage level translator of claim 21, wherein said voltage level translator is a negative voltage translator.

25. The voltage level translator of claim 21, wherein said first and second transistors are P-channel transistors.

26. The circuit of claim 21, wherein said first and second pair of transistors are N-channel transistors.

27. The circuit of claim 6, wherein said second voltage level is V_{BB}.

28. The circuit of claim 6, wherein said first voltage level is ground.

29. The circuit of claim 6, wherein said first and second one-shots each provide a low-going pulse.

30. The circuit of claim 2, wherein said first one-shot further comprises:

a first inverter to receive a first control signal from said first transistor;

a second inverter operatively coupled to said first inverter;

a first N-channel transistor comprising a well tie to said second voltage level, the source terminal of said first P-channel transistor being coupled to said first control signal; and

a second N-channel transistor comprising a well tie to said second voltage level, said second N-channel transistor being coupled with said first N-channel transistor, the gate of said second N-channel transistor being coupled to said input signal.

31. The circuit of claim 2, wherein said second one-shot further comprises:

a third inverter to receive a first control signal from said first transistor;

a fourth inverter operatively coupled to said third inverter;

a third N-channel transistor comprising a well tie to said second voltage level, the source terminal of said first N-channel transistor being coupled to said first control signal; and

a fourth N-channel transistor comprising a well tie to said second voltage level, said fourth N-channel transistor being coupled with said third N-channel transistor, the gate of said fourth N-channel transistor being coupled to said a complement of said input signal.

32. A system board, comprising:

a processor;

a memory device operatively coupled to said processor, said memory device comprising a voltage translator circuit, said voltage translator circuit comprising:

a transistor circuitry for receiving an input signal for translating a signal from a first voltage range to a second voltage range; and

a first and second one-shots operatively coupled to said transistor circuitry, said first and second one-shots to provide at least one pulse for translating said input signal from said first voltage range to said second voltage range.

33. The system board of claim 32, wherein said transistor circuitry further comprises a voltage level translator, comprising:

a first transistor operatively coupled to said input signal, said input signal being in said first voltage range, wherein said first one-shot circuit is being driven by said first transistor;

a second transistor to receive a complementary signal of said control signal, said second transistor to drive a second one-shot circuit to provide a second pulse; and

a first pair and a second pair of transistors, each pair being operatively coupled to said first and second transistors, said first and second pairs of transistors to provide a transition of a signal from a first voltage range to a second voltage range.

34. The system board of claim 33, wherein said first voltage range relates to a voltage of V_{CC} to Ground.

35. The system board of claim 33, wherein said second voltage range relates to a voltage of V_{CC} to V_{BB}.

36. The system board of claim 33, wherein said first one-shot further comprises:

a first inverter to receive a first control signal from said first transistor;

a second inverter operatively coupled to said first inverter;

a first N-channel transistor comprising a well tie to said second voltage level, the source terminal of said first N-channel transistor being coupled to said first control signal; and

a second N-channel transistor comprising a well tie to said second voltage level, said second N-channel transistor being coupled with said first N-channel transistor, the gate of said second N-channel transistor being coupled to said input signal.

37. The system board of claim 33, wherein said second one-shot further comprises:

a third inverter to receive a first control signal from said first transistor;

a fourth inverter operatively coupled to said third inverter;

a third N-channel transistor comprising a well tie to said second voltage level, the source terminal of said first N-channel transistor being coupled to said first control signal; and

a fourth N-channel transistor comprising a well tie to said second voltage level, said fourth N-channel transistor being coupled with said third N-channel transistor, the gate of said fourth N-channel transistor being coupled to said a complement of said input signal.

38. The system board of claim 32, wherein said system board comprises a printed circuit board.

39. A method for performing a voltage translation of a signal, comprising:

providing a transistor circuitry for receiving an input signal for translating a signal from a first voltage range to a second voltage range; and

providing a first and a second one-shot operatively coupled to said transistor circuitry, providing at least one pulse for translating said input signal from said first voltage range to said second voltage range.

40. The method of claim 39, further comprising activating said first one-shot using said input signal.

41. The method of claim 39, further comprising activating said second one-shot to produce an output signal in said second voltage range.

42. A memory device comprising a voltage translator circuit, said voltage translator circuit comprising:

a transistor circuitry for receiving an input signal for translating a signal from a first voltage range to a second voltage range; and

a first and second one-shots operatively coupled to said transistor circuitry, said first and second one-shots to provide at least one pulse for translating said input signal from said first voltage range to said second voltage range.

43. The memory device of claim 42, wherein said transistor circuitry further comprises:

a first transistor operatively coupled to said input signal, said input signal being in said first voltage range, wherein said first one-shot circuit is being driven by said first transistor;

a second transistor to receive a complementary signal of said control signal, said second transistor to drive a second one-shot circuit to provide a second pulse; and

a first pair and a second pair of transistors, each pair being operatively coupled to said first and second transistors, said first and second pairs of transistors to provide a transition of a signal from a first voltage range to a second voltage range.

44. The memory device of claim 43, wherein said first voltage range relates to a voltage of V_{CC} to Ground.

45. The memory device of claim 44, wherein said second voltage range relates to a voltage of V_{CC} to V_{BB}.

46. The memory device of claim 42, wherein said first one-shot further comprises:

a first inverter to receive a first control signal from said first transistor;

a second inverter operatively coupled to said first inverter;

a first N-channel transistor comprising a well tie to said second voltage level, the source terminal of said first N-channel transistor being coupled to said first control signal; and

a second N-channel transistor comprising a well tie to said second voltage level, said second P-channel transistor being coupled with said first N-channel transistor, the gate of said second P-channel transistor being coupled to said input signal.

47. The memory device of claim 42, wherein said second one-shot further comprises:

a third inverter to receive a first control signal from said first transistor;

a fourth inverter operatively coupled to said third inverter;

a third N-channel transistor comprising a well tie to said second voltage level, the source terminal of said first N-channel transistor being coupled to said first control signal; and

a fourth N-channel transistor comprising a well tie to said second voltage level, said fourth N-channel transistor being coupled with said third N-channel transistor, the gate of said fourth N-channel transistor being coupled to said a complement of said input signal.